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Docket No.: P2001,0387

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By: Markus Nolff Date: December 15, 2003

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applic. No.	: 10/715,019
Applicant	: Gabriele Fichtl, et al.
Filed	: November 17, 2003
Docket No.	: P2001,0387
Customer No.	: 24131

CLAIM FOR PRIORITY

Commissioner for Patents,
P.O. Box 1450, Alexandria, VA 22313-1450

Sir:

Claim is hereby made for a right of priority under Title 35, U.S. Code, Section 119, based upon the European Patent Application 011 13 838.5, filed June 6, 2001.

A certified copy of the above-mentioned foreign patent application is being submitted herewith.

Respectfully submitted,

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Die angehefteten Unterlagen stimmen mit der ursprünglich eingereichten Fassung der auf dem nächsten Blatt bezeichneten europäischen Patentanmeldung überein.

The attached documents are exact copies of the European patent application described on the following page, as originally filed.

Les documents fixés à cette attestation sont conformes à la version initialement déposée de la demande de brevet européen spécifiée à la page suivante.

Patentanmeldung Nr. | Patent application No. | Demande de brevet n°

01113838.5

Der Präsident des Europäischen Patentamts;
Im Auftrag

For the President of the European Patent Office

Le Président de l'Office européen des brevets
p.o.

I.L.C. HATTEN-HECKMAN

Anmeldung Nr:
Application no.: 01113838.5
Demande no:

Anmeldetag:
Date of filing: 06.06.01
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Anmelder/Applicant(s)/Demandeur(s):

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ALLEMAGNE

Bezeichnung der Erfindung/Title of the invention/Titre de l'invention:
(Falls die Bezeichnung der Erfindung nicht angegeben ist, siehe Beschreibung.
If no title is shown please refer to the description.
Si aucun titre n'est indiqué se referer à la description.)

Method for manufacturing a trench capacitor with an isolation trench

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Description

Method for manufacturing a trench capacitor with an isolation trench

The invention refers to a method for manufacturing a trench capacitor with an isolation trench. The trench capacitor has a collar isolation and is filled and covered with silicon.

Trench capacitors are used to obtain large capacitances, preferably for DRAMs (Dynamic Random Access Memories) in the form of stand-alone devices or of embedded memory. The trench capacitor is formed within a deep trench within the semiconductor substrate which has single crystal structure. One of the electrodes of the trench capacitor is the doped semiconductor substrate, the other electrode or the storage node of the memory cell is arranged within the trench and is separated from the first electrode by a dielectric layer. The storage node and the two electrodes are situated in the lower section of the trench directed to the bulk substrate. The memory cell further comprises an access transistor which is arranged near the surface of the semiconductor substrate. In order to isolate this so-called active area from the trench capacitor, the first electrode of the capacitor within the substrate is confined by a buried doping area in a vertical direction; and seen a in horizontal direction, the inner electrode made of polysilicon of the capacitor is surrounded by a vertical isolation layer, a so-called collar isolation, preferably a collar silicon oxide.

During the manufacturing of a memory device, first the trench capacitor is manufactured, then the active areas are manufactured. In known capacitor arrangements, two deep trench capacitors are arranged closely together. The active areas of the respective memory cells are situated on the outer area of the double arrangement of the trench capacitors rather than in-between the two trench capacitors. The upper part in-

between the trench capacitors, e. g. reaching from the middle of the first trench and passing over one side of the collar isolation of the first trench capacitor over the silicon substrate and over the collar isolation of the opposing side of the second trench capacitor into the middle of the second trench capacitor. This isolation separates the upper part of the two trench capacitors which are situated closely together. The outer parts of the upper section of the collar isolation are modified to obtain a contact from the active area to the inner electrode of the trench capacitor.

The above-mentioned isolation between the two opposing sides of the trench capacitors is achieved by a shallow trench that covers the upper ends of the two capacitors in the area reaching from between approximately the middle of the inner electrode of the first capacitor to the middle of the inner electrode of the second capacitor. For etching the combination of polysilicon and collar isolation, preferably collar oxide and single crystal silicon, it has to be considered that the material to be etched is a combination of silicon material and isolation material which appear on the horizontal surface to be etched. The etching process must take into account the different properties of the collar isolation and the silicon that are exposed to the etching gases simultaneously. Due to the different etch selectivities of the etching gases within the reactor, it is a challenge to obtain a smooth and flat surface on the bottom of the shallow isolation trench especially as the hard mask that patterns the surface of the semiconductor wafer is typically an oxide or a BSG (Boron Silicate Glass). It is therefore difficult to etch the collar oxide without eroding the hard mask on top of the wafer.

In a conventional etch process flow for etching the shallow isolation trench into the top part of a trench capacitor with collar isolation there is selectivity during the step of etching of silicon so that the collar oxide is less etched

than the silicon. As a result, the collar oxide is still present and is projecting out of the bottom of the already etched shallow trench. Then, the collar oxide has to be removed by an additional process step. As a preceding step, the hard mask must be opened.

It is an object of the invention to provide a method for manufacturing a trench capacitor with a shallow trench isolation in its top part with the trench capacitor having a collar isolation, that requires only few etch steps to obtain the isolation trench whereby the bottom surface of the trench is substantially flat and even.

This objective is solved by a method for manufacturing a trench capacitor with an isolation trench Method for manufacturing a trench capacitor with an isolation trench, comprising the steps of manufacturing of a trench capacitor arranged within a semiconductor substrate, the trench capacitor comprising a lower part having a first outer electrode and a second inner electrode and a dielectric arranged between the first and the seconds electrodes; an upper part having a collar isolation on the sidewalls of the trench, whereby a silicon layer covers the trench capacitor on top of the collar isolation and a hard mask covers the silicon layer;
the method further comprising the steps of opening the hard mask so that a surface of the silicon layer is reached; in a first step, dry etching with an etch gas comprising chlorine or bromine as long as the collar isolation is reached; in a second step, subsequently performing dry etching with an etching gas comprising silicon fluoride.

The method according to the invention requires only two etching steps with different etch chemistry. In addition, the hard mask has to be opened by a conventional etch step in advance. The etching gases for the first step comprise chlorine or bromine. The etch chemistry is maintained up to a depth when the collar isolation is reached. Then the etch chemistry

is changed to silicon fluoride (SiF_4) based chemistry in order to finalize the etching up to the desired depth. Chlorine chemistry is known to etch silicon or polysilicon selectively to oxide or BSG. As a result, the hard mask being made of oxide or BSG is not eroded and the etching of the silicon and polysilicon on top of the trench capacitor advances fast. In the second etch step, SiF_4 is known to etch silicon and isolation material like silicon oxide and silicon nitride with almost no selectivity to each other. But the use of SiF_4 in combination with oxigen (O2) has the advantage that by-products, e. g. silicon oxide, are formed that deposit onto the hard mask on top of the wafer. As a result, the bottom of the trench is etched conformly, thereby obtaining a plain and flat bottom of the trench. Although the silicon fluoride based etch chemistry is almost equally etching silicon and oxides, isolation material, or BSG, the deposition on the top surface of the wafer onto the hard mask maintains the hard mask. Moreover, there is an equilibrium of etching and deposition on the top surface of the hard mask so that the mask is substantially maintained and is not deteriorated by erosion. In contrast, within the trench, especially on the bottom surface of the trench, the silicon oxide by-products are not present due to the low amount of oxide in the bottom of the trench so that there is substantially no deposition on the bottom of the trench. In the bottom of the trench, the etching of silicon, polysilicon, and silicon oxide that forms the collar isolation proceeds at substantially the same etch rate.

The etching gases for the first step, i. e. chlorine or bromine-based, can be hydrogen chlorine (HCl) or chlorine (Cl_2) and may be diluted by helium (He) or oxygen (O_2). The etch gases during the second etch step comprise SiF_4 as already disclosed and may additionally contain CF_4 (carbontetrafluoride). The etch gases in the second step may further be diluted by oxygen (O_2) and/or argon (Ar).

In order to switch from the first etch chemistry to the second etch chemistry, a measurement is performed that detects the etching of the collar isolation or collar oxide through the detection of the generated by-products. The measurement technique may be optical emission spectroscopy. Alternatively, interferometry can also be used. As a further alternative, the transition from the first etch chemistry to the second etch chemistry can be determined by a time measurement. The optimal time period which is necessary to reach the upper part of the collar isolation can be determined by experiments in advance. This time is pre-set for the production run and the switch from the first to the second etch chemistry is made when the pre-set time has lapsed.

The collar isolation may be made of a collar oxide, preferably a silicon oxide. The hard mask is made of BSG or is made of an oxide, preferably silicon oxide.

The shallow isolation trench is used to isolate the top part of two deep trench capacitors from one another which are located closely side by side to one another. The opposing parts of the collar isolation are removed whereas the not opposing outer parts of the collar oxide are maintained. The isolation trench seen from the top starts within the inner polysilicon electrode of the trench capacitor and extends over the collar oxide of this capacitor, over the silicon between the two capacitors of the semiconductor substrate, over the collar oxide of the neighbouring adjacent trench capacitor ending within the polysilicon of its inner electrode.

The invention will now be described in detail in connection with the drawings.

Figure 1 shows a cross-section through a semiconductor wafer with two neighbouring trench capacitors with the hard mask already opened.

Figure 2 shows the same portion of the cross-section after the first etching step.

Figure 3 shows the cross-section after the completion of the etching process.

The cross-section depicted in figure 1 shows a silicon substrate 10 with two capacitors 20, 30 almost completed at this manufacturing stage. The capacitors are deep trench capacitors, several millions of them arranged regularly on a DRAM device. The capacitors 20, 30 are grouped together. The capacitor 30 is explained in detail, the capacitor 20 has a corresponding structure. The capacitor 30 has a lower part 34 and an upper part 35. The lower part 34 is the storage node that stores an electric charge. The lower part 34 comprises a first electrode 341 within the substrate, a dielectric layer 342 arranged on the walls of the trench and an inner electrode 343 filling the lower part 34 of the trench. The dielectric material 342 is silicon nitride. The upper part 35 of the trench capacitor 30 has a collar oxide 31, 32 that isolates the inner electrode 33 from the substrate 10. Close to the right end of the capacitor 30, the access transistor for the memory cell will be formed later on. The described structure is mirrored to the other capacitor 20. Both capacitors 20, 30 are arranged closely together with no active areas in-between, but to the left side of capacitor 20 and the right side of capacitor 30. In order to isolate the two capacitors from each other, a shallow isolation trench 50 must be formed into the substrate and into the capacitors 20, 30 by a dry etching process. The etching process has to etch the physician of the innerdectrode of the capacitor, the collar oxide and the single crystal silicon of the bulk silicon between the capacitors at the same time.

The wafer is already covered with an epitaxial layer of silicon. The inner electrodes 23, 33 of the trench capacitors are filled with polysilicon. The semiconductor substrate 10 is

also made of silicon. The cross-section depicted in figure 1 shows a PAD-nitride 42 and a hard mask 40 on top of the epitaxial silicon layer. The hard mask 40 is made of BSG (Boron Silicate Glass) or may be a silicon oxide. The hard mask 40 has already been patterned during a preceding hard mask open etch step. The opening 41 into the hard mask layer 40 provides a mask for the subsequent etching process steps. The hard mask opening is performed by conventional methods. The process of the invention starts after the hard mask was already opened when the surface 43 of the epitaxial silicon layer is already free.

In a first etching step, the end of which is shown in figure 2, the polysilicon and silicon material 12 within the mask open section 41 is removed by dry etching. The etch step is performed in a dry etching tool, for example a DPS-chamber from Applied Materials Inc. The etch chemistry within the reactor is selected to be highly selective with respect to silicon in order to remove the silicon layer 12 within the open portion 41 of the hard mask. The etch chemistry for the first step is based on chlorine or, alternatively, on bromine. The etch chemistry can include HCl and Cl_2 or, alternatively, HBr. The etch chemistry can be diluted with He or O_2, or with a combination of He and O_2. These etch gases provide for a high-selective silicon etch so that silicon 12 is easily etched whereas the hard mask 40, being made of oxide or BSG, is maintained and is not subject to any erosion.

This first etch step uses etch chemistry that is highly selective to oxide, so that silicon is etched. The first etch step is performed until the top part of the collar oxides 22, 31 of the adjacent trenches 20, 30 is reached, as is shown in figure 2. This point of the etch process can be detected by a measurement employing interferometry or optical emission spectroscopy. Alternatively, the state shown in figure 2 can be determined by a monitoring of the etching time. In previous experiments a pre-determined time can be defined that is

sufficient for the etching process to reach the top part of the collar isolations. The status of the etching process shown in figure 2 can be reached after etching the wafer for a time period equal to the pre-determined etching time.

After reaching the oxide material of the collar isolation 22, 31, the etch chemistry has to be changed so that the silicon, also including the collar isolation, are etched. By reaching the status shown in figure 2, the etch chemistry within the chamber is changed to a SiF_4 base also containing O_2. SiF_4/O_2 is known to etch oxide and silicon at substantially the same rate. The etch chemistry during the second etch step now starting may further contain CF_4. The etch chemistry may be diluted with Ar. The SiF_4 based etch chemistry is known to generate SiO_2 by-products when etching oxide or BSG. The silicon oxide by-products deposit mainly on the hard mask since the concentration of the by-products is rather high. Since the silicon material dominates at the bottom 52 of the trench, there is no substantial silicon dioxide by-product in this area. Therefore, the etch process continues to etch deeper into the semiconductor wafer since substantially no deposition of silicon oxide takes place on the bottom 52 of the isolation trench. In contrast, an equilibrium of deposition and etching is established in the area of the BSG or silicon oxide hard mask. As a result, the etch process advances within the trench without substantially eroding the hard mask.

The process flow according to the invention results in a substantially flat and even bottom surface 52 of the isolation trench with a two-step process only. There is no need to change the process chamber. Only the etch chemistry has to be changed from chlorine or bromine-based etch chemistry during the first step to SiF_4/O_2-based chemistry during the second step after reaching the collar isolation. The process flow according to the invention is preferably valuable for smaller feature sizes in highly integrated DRAMs. The trend is to

have an isolation trench of smaller width and larger depth, so that the aspect ratio of the trench increases. The process according to the invention is of particular value for feature sizes of 0.14 µm (micrometer) and below.

After the end of the shallow isolation trench etch the trench is filled with isolation material, e. g. silicon oxide. Further, the so-called active areas including the access transistor of the memory cell, the connection of the access transistor to the inner polysilicon electrode of the trench, and finally, word and bit lines are formed.

The isolation trench only covers the opposite, neighbouring collar isolations 22, 31 of the two trench capacitors 20, 30. The not opposing collar oxides 21, 32 are left unchanged. The sidewall of the trench ends within the polysilicon material of the inner electrode of the trench, approximately in the middle of the trench electrode. Thereby, both trench capacitors and memory cells are isolated from each other.

The new process flow reduces the number of steps to two due to a combined deposition/etch step within an ICP (Inductive Coupled Plasma) type etch chamber. Compared to other methods, there is no separate step required to remove the collar isolation. As an advantage of the invention, the top side polysilicon material is etched with a highly selective polysilicon etch chemistry and the collar isolation as well as the polysilicon are etched later with a surface-protecting chemistry that establishes an equilibrium of erosion/deposition on the hard mask rather than an etch only behaviour within the isolation trench. The deposition behaviour during the second etch step predominates on the top, whereas the bottom of the trench is predominantly etched.

The process parameters in the etch chamber, e. g. a DPS etch chamber from Applied Materials Inc., during the first and the second etch steps are as indicated in the table below. The

parameters include the power for the upper inductive coil of the etch chamber and the power for the lower inductive means which performs a bias power applied to the wafer chuck. The parameters further comprise approximate values for flow rates in units of sccm for the etch gases to be introduced into the chamber.

	Source power	bias power	Pres-sure	Cl_2	HCl	He/O_2	CF_4	O_2	SiF_4	Ar
	in W	in W	in mTorr	in sccm	in sccm	in sccm	in sccm	in sccm	in sccm	in sccm
1st step	550	350	4	30	120	15	-	-	-	-
2nd step	2,500	200	6	-	-	-	61	45	45	150

The numbers given above may vary by a range of ±10% and apply to etch tools having reaction chambers for wafers of a size of 300 mm.

List of reference numerals

10	silicon substrate
12	silicon layer
20, 30	trench capacitor
21, 22, 31, 32	collar oxide
33	inner electrode
34	lower part of trench capacitor
35	upper part of trench capacitor
341	first electrode
342	dielectric
343	inner electrode
40	hard mask
41	hard mask open
42	pad-nitride
43	silicon layer surface
50	isolation trench
51, 52	bottom of isolation trench

Claims

1. Method for manufacturing a trench capacitor with an isolation trench (50), comprising the steps of:
- manufacturing of a trench capacitor (20, 30) arranged within a semiconductor substrate (10), the trench capacitor comprising:
- a lower part (34) having a first outer electrode (341) and a second inner electrode (343) and a dielectric (342) arranged between the first and the second electrodes;
- an upper part (35) having a collar isolation (31, 32) on the sidewalls of the trench, whereby a silicon layer (12) covers the trench capacitor on top of the collar isolation (31, 32) and a hard mask (40) covers the silicon layer (12);
the method further comprising the steps of:
- opening the hard mask (40) so that a surface of the silicon layer (12) is reached;
- in a first step, dry etching with an etch gas comprising chlorine or bromine as long as the collar isolation (22, 31) is reached;
- in a second step, subsequently performing dry etching with an etching gas comprising silicon fluoride and oxygen.

2. Method according to claim 1,
c h a r a c t e r i z e d in that
the etching gas of the first step comprises the gases hydrogen chlorine and at least one of the gases helium and oxygen.

3. Method according to claim 1,
c h a r a c t e r i z e d in that
the etching gas during the first step comprises the gas hydrogen bromine and at least one of the gases helium and oxygen.

4. Method according to one of claims 1 to 3,
c h a r a c t e r i z e d in that

the etching gas during the second step further comprises the gases argon.

5. Method according to claim 4,
c h a r a c t e r i z e d in that
the etching gas during the second step further comprises the gas CF_4.

6. Method according to one of claims 1 to 5,
c h a r a c t e r i z e d in that
the first etching step is finished and the second etching step is started when during the first step a by-product generated from the oxide isolation is detected.

7. Method according to one of claims 1 to 5,
c h a r a c t e r i z e d in that
the first etching step is finished and the second etching step is started in response to a signal obtained from a measurement employing interferometry or a measurement employing optical emission spectroscopy.

8. Method according to one of claims 1 to 5,
c h a r a c t e r i z e d in that
the second etching step is started after performing the first step during a predetermined time period.

9. Method according to any of claims 1 to 8,
c h a r a c t e r i z e d in that
the hard mask (40) comprises boron silicate glass.

10. Method according to any of claims 1 to 8,
c h a r a c t e r i z e d in that
the hard mask (40) comprises silicon oxide.

11. Method according to any of claims 1 to 10,
c h a r a c t e r i z e d in that
the collar isolation (22, 31) comprises silicon oxide.

12. Method according to any of claims 1 to 11, c h a r a c t e r i z e d in that the semiconductor substrate (10) comprises at least two trench capacitors (20, 30) having a collar isolation (21, 22, 31, 32) that are arranged in close vicinity and in that the hard mask (40) is arranged relative to the at least two trench capacitors (20, 30) so that portions of the collar isolations (22, 31) that are facing each other are being etched during the second etching step and in that portions (21, 32) of the collar isolations that are not facing each other are maintained during the second etching step.

Abstract

Method for manufacturing a trench capacitor with an isolation trench

A method for manufacturing a trench capacitor comprises the step of etching a shallow isolation trench in a two-step process flow. During the first etching step, an etch chemistry based on chlorine or bromine performs a highly selective etch for silicon (12). During the second step, the etch chemistry is based on SiF_4 and O2 which rather equally etches polysilicon (12) and the collar isolation (22, 31). On top of the wafer, the deposition of silicon oxide on the hard mask (40) predominates and avoids an erosion of the hard mask (40). On the bottom (52) of the trench (50) the conformal etching of polysilicon (12) and collar isolation (22, 31) predominates. The method provides an economic process flow and is suitable for small feature sizes.

Figure 3

FIG. 2

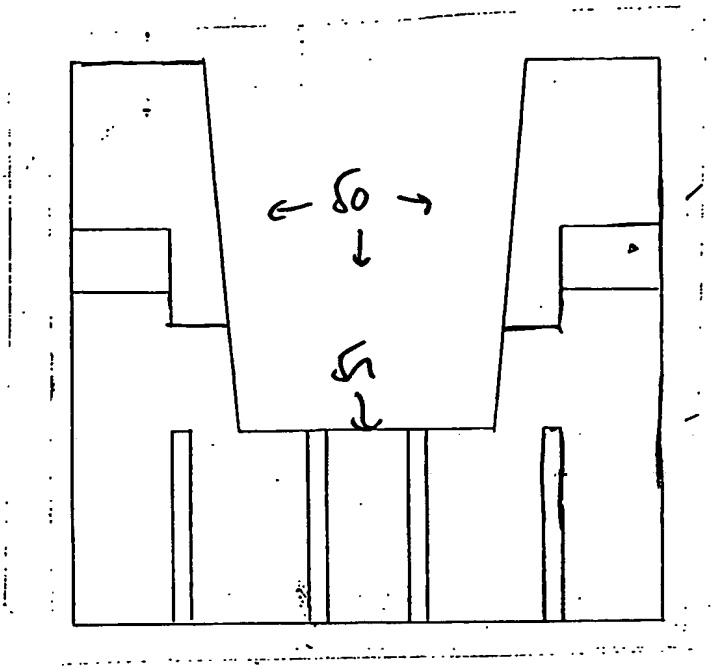

FIG. 3

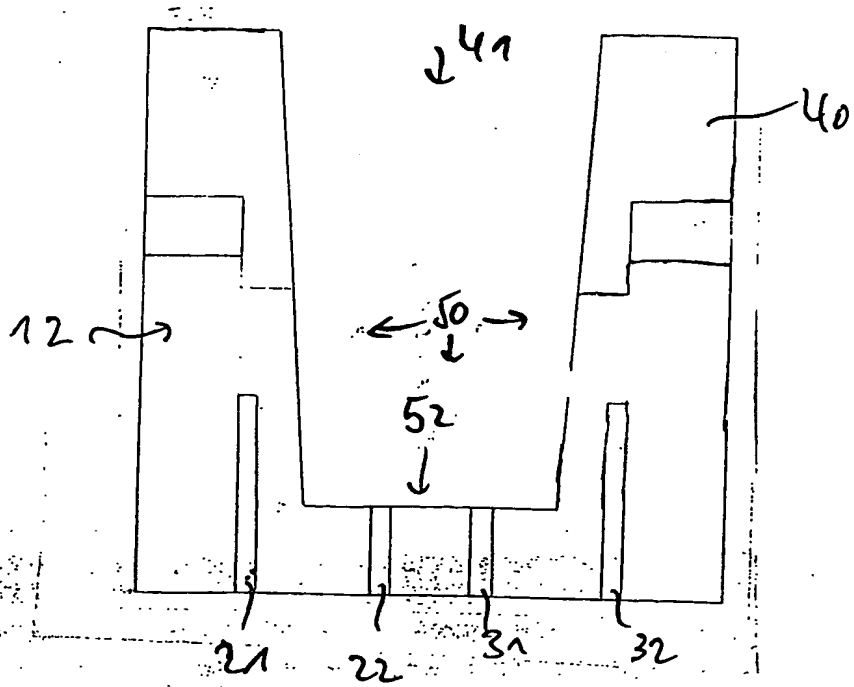

Fig. 1